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# BIST for Memory with Address and Syndrome Compression

**Ajinkya R. Kapse[1], Poorvi K. Joshi[2]**

Student, Dept of Electronics, RCOEM, Nagpur, India [1]

Assistant Professor, Dept of Electronics, RCOEM, Nagpur, India [2]

**Abstract**: Because of fixed number of pins, buit-in self-test (BIST) for embedded RAMs ordinarily sends out the diagnostic information serially, which increases the total diagnostic time. The proposed BIST decrease the diagnostic time by lessening number of bits required for sending out defective address and fault syndrome. The fault address bits are diminished by sending out differential address and fault syndrome is compressed utilizing march element based (MEB) compression. Simulation results demonstrate that the compression ratio is around 43.01% for a 4K×16-bit memory.

**Keywords**: Random Access Memories; built-in self-test; diagnosis; compression

## I. INTRODUCTION

Memories are broadly utilized cores in system on chips (SOC). Memory cores typically are involved in vast part of chip. The yield of the chip is influenced by the defects in the memory cores. In this way analysis of memory is imperative as to enhance the yield of the chip. For testing and diagnosis of embedded RAMs Built-in self-test (BIST) procedures are utilized. Because of constraint in pin-count, the diagnostic information is sent out serially, which is a time expending process. A few strategies has been proposed in [1]-[8] to diminish the exportation time by compacting the diagnostic information. There are for the most part two sorts of systems in which diagnostic information is compacted, first is the pause and export way and second is at-speed diagnostic data compression. In at-speed diagnostic information compression strategies the information exportation is in lossy form so the exact bitmap can't be developed from this information.

In a nano-scale RAM because of increase in interconnection in various layers resistive open deformities have expanded [9]. These imperfections are mainly because of resistive-open vias [10]. The resistive open imperfections cause dynamic faults. At nano-scale dynamic faults have turned into an essential class of faults. To detect timing related faults March test are applied having number of read operation in a March element. While testing utilizing traditional pause and way the March test for dynamic fault is not effective. Additionally, when static fault happen excess diagnostic information is sent out. The March-element based (MEB) compression can minimize the redundancies furthermore distinguish the dynamic faults. With increase in the size of RAM the location bits required additionally increments. Therefore, to export address bits additional time is required. The address bits can be compressed by utilizing differential address. In this article we set forward a BIST architecture compress fault address utilizing differential address and evacuate redundancies utilizing March-element based (MEB) compression.

## II. PRELIMINARY AND MOTIVATION

In memories different faults are modelled as functional faults. The faults are mainly divided into two types i.e. static and dynamic faults. At most one read operation is required to detect the static fault and dynamic fault are detected by more than one read operation. To identify functional faults in RAMs March test are utilized. Various March elements are present in a March test which are enclosed bracket. Each March element has number of test operation with an address direction which can increase (⇑), decrease (⇓) or in any direction (⇕). For instance, March B-test {⇕ (w0); ⇑ (r0, w1, r1, w0, w1); ⇑ (r1, w0, w1); ⇓ (r1, w0, w1, w0); ⇓ (r0, w1, w0)} is utilized for detecting static faults in RAM, where rx indicate read operation with expected output x and wx signify write operation with input x. A March test for identifying dynamic faults has various read operations. For example, March DD [11] test {⇕ (w0); ⇑ (r0, w1, w1, r1, w1, w1, r1, w0, w0, r0, w0, w0, r0, w0, w1, w0, w1); ⇑ (r1); ⇑ (r1, w0, w0, r0, w0, w0, r0, w1, w1, r1, w1, w1, r1, w1, w0, w1, w0, r0); ⇑ (r0); ⇓ (r0, w1, r1, w1, r1, r1, r1, w0, r0, w0, r0, r0, r0, w0, w1, w0, w1); ⇑ (r1); ⇓ (r1, w0, r0, w0, r0, r0, r0, w1, r1, w1, r1, r1, r1, w1, w0, w1, w0, r0); ⇑ (r0)} can be utilized for recognizing static and dynamic faults.

For supporting memory diagnosis, the BIST circuit exchanges the diagnostic information with automatic test equipment (ATE). The Diagnostic information comprise of faulty location, session number and hamming syndrome. The session number gives information about the read operation of the March element that has detected a fault. The location of the defective word is given by the fault address. The bitwise XOR of expected and read information is the hamming syndrome. It demonstrates which bit in the faulty word has a defect. For the most part, a BIST sends out diagnostic information by pause and export (PAE) way. In PAE after a fault is detected the BIST is paused and afterward diagnostic information is sent out. The BIST continues its operations after the

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exportation is finished. However, when a March element having more than one read operations is applied to a BIST having PAE way every read operation may produce same hamming disorder and henceforth same diagnostic information is sent out numerous times. To defeat this issue MEB [1] compressions is a compelling way. In this the excess information is sent out just once. In this way when a fault is spotted hamming syndrome of the fault is compared with the previous hamming syndromes of the specific March element which are put away in a small content addressable memory (CAM).

If the hamming syndrome is distinct the new hamming syndrome is put away in another address in CAM, yet in the event that it is same it is not stored. The diagnostic information exportation process begins after the last test operation in the March element is over.

The MEB Compression scheme compress the excess hamming syndrome yet the faulty location which is long if the RAM size is extensive. The fault location can be compressed by sending differential location rather than full address [8]. To accomplish more compression and lessen diagnostic exportation time we propose a BIST which evacuate the excess hamming syndrome by MEB compression and decreases address bits by utilizing differential address technique.

## III.PROPOSED BIST ARCHITECTURE

### A. BIST Architecture

The proposed BIST outline is shown in fig 1. It has three primary components controller, test pattern generator and compressor unit. The controller interfaces the BIST with the automatic test equipment (ATE). The controller takes commands serially in from the ATE and offers it to the test pattern generator (TPG). The TPG gets the commands and preforms read/write operation of March test on the RAM as indicated by the received commands.

The compressor gathers and compares the hamming syndromes related of the specific address of March element. At that point compressor joins the compacted hamming syndrome with the differential address and differential ID and exports the diagnostic information out to the TPG.

The IO associated with the BIST design includes clock (clk), command serial input (si_in), reset (rst), shift enable (sft_en), test done (test_done), mode select (ms), error signal (err) and serial output (si_out). The mode select signal (ms) is passed down to toggle RAM between the normal mode of operation and the test mode of operation. When sft_en signal is high the BIST receives commands serially from si_in signal.

When a command is executed completely the test done signal becomes and the BIST stops and waits for next command. When an error is detected by the BIST and BIST wants to export the diagnostic data out to the ATE err signal becomes high. The data is exported from the signal si_out. high. The information is sent out from the sign si_out.

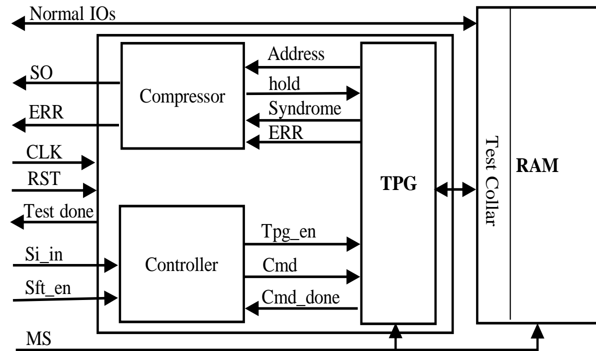


Figure 1 Block Diagram of BIST

### B. Design of TPG

The main purpose of TPG is to generate different signals to perform operations on the RAM. The TPG receives command from the controller. These command are nothing but the March element which is to be applied. Multiple commands are required to perform operations of the March element. Fig. 2 shows the state diagram of TPG.

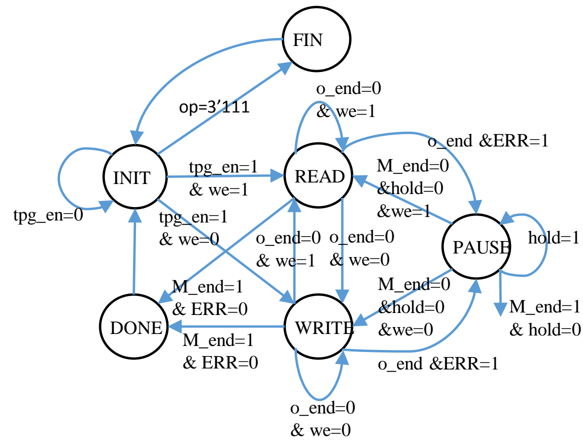


Figure 2 State diagram of TPG

At the beginning the TPG is in initial mode when tpg_en=0. When tpg_en=1 the tpg receives the first command from the controller and performs read/write operation according to the command. If we=0 write operation is performed and if we=1 read operation is performed. The o_end=1 signal denotes the last operation of the March element is reached.

If an error is detected by a read operation the ERR signal becomes high. After the final operation of March element is performed and if err signal is high the test pattern generator goes to the pause state and the controls are given to the compressor. If all operations are performed the test pattern generator goes to the done state. When the command received from the controller is a null command (op=3’111) the TPG goes to finish state and the test done signal is made high.

### C. Design of Proposed Compressor

The simplified block diagram of proposed compressor is shown in Fig. 3. When an error is detected by the test pattern generator unit sends the hamming syndrome of the spotted fault to the compressor.

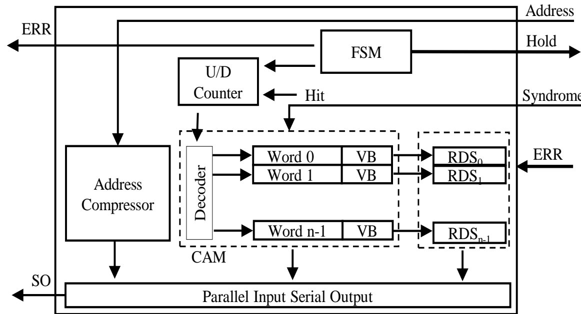


Figure 3 Block diagram of the proposed BIST

The compressor compares the received hamming syndrome with the previously stored syndromes if the syndrome does matches with the existing one the syndrome is stored in a new location in the CAM. If the new syndrome matches to one present in the CAM the RDS (Read Detection Status) is updated. RDS gives information about which read operation detected fault. For instance, if four read operations are there in a March element and second operation detects the fault the then RDS will be 0100. When all operations of the March element are performed and if errors are detected differential id and differential address are calculated according to previous faulty address. Fig. 4 shows how differential address are calculated.

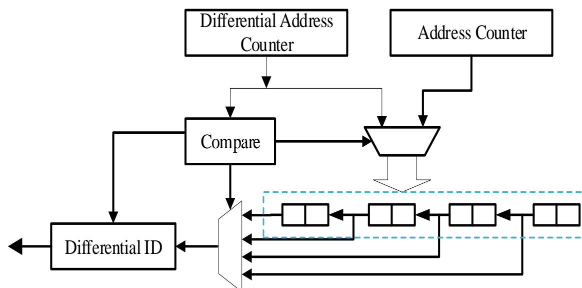


Figure 4 Address Compressor

The counter gives the differential address and a comparator compares it and calculates the differential ID. First the differential address and differential ID of the faulty address is exports serially then the hamming syndrome related to the fault are exported one by one from the CAM. The valid bit of the last hamming syndrome is made high which denotes the end of the data exportation.

## IV. EXPERIMENTAL RESULTS

This segment analyses the compression ratio of the proposed scheme. The ratio of number of bits of the compressed diagnostic data to that of number of bits of the original diagnostic data is defined as the compression ratio.

$$Compression\ ratio = \frac{No.of\ Compressed\ bits}{No.of\ Orignal\ bits}$$

Following are the wave forms for simulation of the proposed BIST with and without faults.

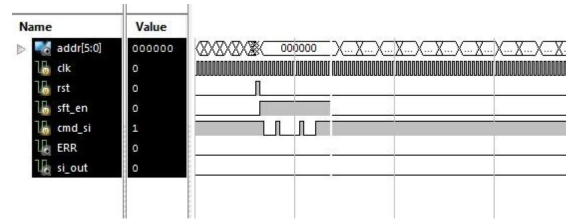


Figure 5 Simulation waveform without faults

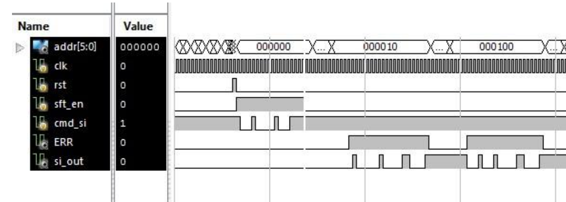


Figure 6 Simulation waveform with faults

It can be seen from the waveform that when the fault is detected by BIST the ERR signal becomes 1 and si_out signal exports the diagnostic data.

To calculate the compression ratio of the proposed scheme different RAM were designed having different sizes of 64 x 16, 256 x 16, 1024 x 16 and 4096 x 16. The memory word size is kept constant i.e. 16. Poisson fault distribution with mean 7.8 was used. In each RAM 70% static faults and 30% dynamic faults were injected. For dynamic faults 80% of them are detected by 2 consecutive read operations and 20% are detected by 3 consecutive read operations. Table I show the results of the simulation. Our results are compared with that of MEB compression scheme. March DD was used to test the RAMs, it can detect both static as well as dynamic faults.

Table I
Diagnostic Data Compression Ratio for Different RAM Configurations

| March Algorithm | March DD [11] | |
|---|---|---|
| Mean | 7.8 | |
| RAM configuration | [1] | Ours |
| 64 x 16 | 47.77 | 48.01 |
| 256 x 16 | 47.08 | 46.11 |
| 1024 x 16 | 46.52 | 44.45 |
| 4096 x 16 | 46.04 | 43.01 |

Table II, III and IV shows Comparison results for different fault distributions, where c, r and clus denotes column, row and cluster faults for different March test used.

Table II
Comparison Results for Different Fault Distributions for March AB test

| RAM configuration | 8k x 16 bit | | |
|---|---|---|---|
| March Algorithm | March AB | | |
| Scheme | c: 0%<br>r: 0%<br>clus: 0% | c: 0%<br>r: 0%<br>clus: 40% | c:10%<br>r:10%<br>clus: 0% |
| MEB Compression | 78.78% | 77.57% | 78.98% |
| Proposed Compression | 67.35% | 66.46% | 67.01% |

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Table III
Comparison Results for Different Fault Distributions for March MD2 test

| RAM configuration | 8k x 16 bit | | |
|---|---|---|---|
| March Algorithm | March MD2 | | |
| Scheme | c: 0%<br>r: 0%<br>clus: 0% | c: 0%<br>r: 0%<br>clus: 40% | c:10%<br>r:10%<br>clus: 0% |
| MEB Compression | 41.29% | 40.31% | 39.40% |
| Proposed Compression | 35.23% | 34.45% | 31.35% |

Table IV
Comparison Results for Different Fault Distributions for March DD test

| RAM configuration | 8k x 16 bit | | |
|---|---|---|---|
| March Algorithm | March DD | | |
| Scheme | c: 0%<br>r: 0%<br>clus: 0% | c: 0%<br>r: 0%<br>clus: 40% | c:10%<br>r:10%<br>clus: 0% |
| MEB Compression | 45.23% | 43.24% | 44.33% |
| Proposed Compression | 38.96% | 37.8% | 36.78% |

## V. CONCLUSIONS

As more and more memory cores are embedded in state-of-the-art SOCs, embedded memory testing has emerged as a key issue in the VLSI design, implementation and fabrication flow. One of the key issue is to tackle the problem of testing time, compression of diagnostic data i.e. fault address and is an effective to reduce the testing time. It is important to reduce the testing time so as to reduce the cost of manufacturing. The proposed compression techniques can be used to speed up the transmission of diagnostic data. Compression ratio improves as the RAM size increases. This is because of the fact that proposed compression scheme includes differential address compression. For memory having cluster, column and row decoder faults compression ratio improves more.

The proposed design reduces the diagnostic data exportation time as it compresses both address as well as remove the redundant hamming syndrome. The design is optimum where the RAM size is large having long address bits. The design can be used to detect static as well as dynamic faults. For the March Test having ability to detect static as well as dynamic faults the proposed design gives better compression ratio as compared to the March Test having ability to detect only static faults.

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